From Sand to Silicon Wafer
Introduction

- Introduction
- Silicon
- Production of technological Silicon
- Production of monocrystalline Silicon
- Si-Wafer production
- Future requirements
Siltronic is a leading manufacturer and global supplier of hyperpure, electronic grade silicon to the semiconductor industry.

- 100% part of Wacker Group, Germany
- Global Sales in 2003: 871 Mio EUR
- Capital Investments 164 Mio EUR
- 6158 Employees worldwide
- 14 Sales offices
- 8 Production Fabs in 5 Locations around the World
- Products: Chlorosilanes; polycrystalline silicon, monocrystalline ingots; as cut, lapped, etched, polished, annealed or epitaxial wafers from 100mm to 300mm diameter
Worldwide Production sites

- Portland, Oregon
- USA
- Freiberg
- Singapore
- Hikari
- Japan
- Germany
- Singapore
- Burghausen
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Silicon basics

- Gray, metallically lustrous element
- After Oxygen (50.5%) Si is second most abundant element (27.5%) in the lithosphere
- It does not occur in elemental form, only in oxides and silicates
- First attempt to obtain elementary silicon 1700, isolated from ferrosilicon in 1810 by Berzelius
Different structures of silicon

- Amorphous
- Polycrystalline
- Single crystal
Silicon crystallizes in the diamond structure like diamond or germanium.

Silicon is a nonmetallic, indirect semiconducting element with a resistivity of ca. 400 \( \text{k}\Omega \cdot \text{cm} \) at room temperature in its purest state.

Atoms: \( 5 \times 10^{22} \, /\text{cm}^3 \)

Important Orientation: \(<100>, \,<111>\)
Electrical behaviour

<table>
<thead>
<tr>
<th>Conductors</th>
<th>Semi-conductors</th>
<th>Insulator</th>
</tr>
</thead>
<tbody>
<tr>
<td>(Al, Cu, Mg, ...)</td>
<td>(Si, Ge, ...)</td>
<td>(SiO₂, ...)</td>
</tr>
</tbody>
</table>

- **Conductors**
  - Type I
  - Type II

- **Semi-conductors**
  - ∆E ≈ 1 eV

- **Insulator**
  - ∆E ≈ 8 eV

**Electron-Energy**

- Conduction band
- Valence band
Doping

Silicon

**n-type**

- Additional electrons
- Ionised donators

**Electron-Energy**
- $E_V$
- $E_D$
- $E_L$

**Hole-Energy**
- $E_A$
- $E_E$

**p-type**

- Ionised acceptors
- Additional holes

**Electron-Energy**
- $E_V$
- $E_L$

**Hole-Energy**
- $E_A$
- $E_E$

**Ohmic law**

\[
j = \sigma * E = q * (n * \mu_n + p * \mu_p) * E
\]

- $\mu_n, Si = 1450 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$
- $\mu_p, Si = 450 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$
Doping elements:

- **n-type**: P, As, Sb
- **p-type**: B

Typical spec. resistivity range:

1 mΩcm - >30 Ωcm
Defects in Silicon crystals

**Point-Defects:**

- **Vacancy**
- **Si interstitial**
- **Interstitial, no Si**
- **Substitutional atom**

**Stacking faults**

- **Surface stacking faults**
- **Bulk stacking faults**
- **Stacking faults caused by scratches**
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Natural Silicon-dioxide, purity < 90%

Carbothermal reduction of Silicon dioxide

\[ \text{SiO}_2 + 2C \rightarrow \text{Si} + 2\text{CO}; \Delta H_{2100} = +695 \text{ kJ} \]

3% of the world production volume of metallurgical-grade silicon is used for production of electronic applications (el. devices, solar cells, sensors, micromechanics)

Metallurgical grade Silicon, purity: 98% up to 99.99%

From natural Si to metallurgical Si
**From Sand to Silicon Wafer**

**Production of technological Silicon**

**Purification of Si**

**Fluidized Bed Reactor**

- **Si** + **3 HCl** ⇌ **SiHCl₃** + **H₂**
- **Si** + **4 HCl** ⇌ **SiCl₄** + **2 H₂**

**Destillation and stripping columns**

**CVD of polycrystalline Silicon**

- Heat up to 1400 K

**Electronic grade Silicon, purity: > 99,999999%**

**HCl:** Hydrogen chloride  
**SiCl₄:** Silicon tetrachloride  
**SiHCl₃:** Trichlorsilane
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Introduction to single crystal growth

**Floating Zone (FZ)**
- Keck and Golay invented this method
- No crucible is used
- Very low impurity concentration in the material
- FZ material is used for discrete devices and high power devices
- Diameters up to 150 mm in standard production

**Czochralski single crystal growth (CZ)**
- Named after J. Czochralski (1918)
- The CZ Process was modified by Teal and Little (1950)
  - Using a seed to define the crystal orientation
  - Diameter-control by the heating power and pulling rate
  - Control of the doping variation by the crystal rotation and pulling velocity
- Since 1970 the CZ method is the common method for IC applications
- Diameters up to 300 mm in standard production
From Sand to Silicon Wafer

Production of monocrystalline Silicon

View of a CZ growth apparatus
Single steps in CZ growing

Quartz crucible filled with polycrystalline silicon

Heat up to liquid silicon

Crystal neck pulling

Increasing diameter

Crystal pulling

Single crystal silicon after CZ growth
Crystal neck pulling

1. Seed of the proper orientation
2. Diameter reduction
3. High pulling rate and small diameter
4. Crystal neck will be dislocation-free after a few centimeters

Liquid Si at 1700 K
Growth process

Production of monocrystalline Silicon

Schematic view of the growth process

- Crucible (SiO$_2$)
- Melt
- 28 kg - 110 kg
- Crystal rotation axis
- Heat loss
- Heat gain
- Growth interface
- Meniscus
Impurities are absorbed by the silicon melt. Due to segregation effect only a small portion of impurities is incorporated into the crystal. Example: from 100000 iron atoms in the melt only one atom is incorporated into the crystal.

Typical values of impurities in the crystal:
- O: $10^{17}$ at/cm³ - $10^{18}$ at/cm³ (depend on costumer spec)
- C: $< 5 \times 10^{16}$ at/cm³
- Metall impurities (Fe, Al, Ni ...) lower than detection limit or $< 10^{11}$ at/cm³

Due to the segregation effect the concentration of impurities increases with increasing crystal length.
Vacancies and interstitials are moveable at high temperature

Very important to intrinsic Gettering
Future activities

- Increase of diameter, perhaps 400mm and more
- Optimized growth condition —> Perfect Silicon
- Temperature fluctuations at the solid-liquid interface
- Modifying melt flows
  - Growth parameter
  - Crystal rotation rate
  - Crucible rotation rate
  - Melt dimensions
  - Furnace dimensions and design
  - Magnetic fields
- Better resistivity homogenity
- Lower impurity concentrations
- Lower COP (crystal originated Pits)
- Lower BMD (Bulk micro defects)
- Reduction of stacking faults
- Lower resistivity

Computer-simulated CZ-prozess

Procedure 1

Defects due to interstitials
1 \times 10^{14}
Defect free
0

Defects due to voids
2 \times 10^{14}

Procedure 2

/\text{cm}^3
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• **Si-Wafer production**
• Future requirements
1. Surface grinding
2. Sawing
   2.1. Wax-mounting
2.2. Sawing
   2.2.1. ID-Saw
   2.2.2. Wire-Saw
2.3. Tab removal
3. Edge rounding
4. Acid clean
5. Lapping/Grinding
6. Cleaning
7. Laser-Mark
8. Cleaning
9. Acid Etching
10. Thermal anealing
11. Mechanical backside treatment
   11.1. Standard Damage
   11.2. Wetblast
   11.3. Poly-silicon deposition
12. Sealing
   12.1.1. LPCVD
   12.1.2. APCVD
13. Polishing
   13.1. Wax-mounting
13.2. Polishing
   13.3. Wax removal
   13.4. Geometry Measurement
14. Cleaning
   14.1. Pre-cleaning
   14.2. Final-cleaning
   14.3. Surface measurement
15. (Epitaxy)
16. Packaging
Due to segregation effect the ingot is cut in defined lengths for customer resistivity, C, and O spec.

Ground to cylinders of the necessary diameter.

To allow crystal oriented positioning of the wafers flats or notches are ground at special crystallographic sites.

Cut Test-Wafer for C, O, resistivity measurement to check customer requirements.
The ID saw blade is characterised by a thin ring-shaped core, the inner diameter which is designed as a cutting edge.

- Warp
- Thickness variation
- Off-orientation
- Used for diameters from 4" up to 6"
- Up to 24 h to slice one ingot
- Flexible for different wafer thickness

**ID saw blade in detail**

- Core thickness: 150 µm

**Damage due to sawing process**

- as cut wafer
- Polished wafer

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Datum: 13.09.2004
Seite: 28
Wire Saw

- Warp
- Thickness variation
- Off-orientation
- Used for diameters >= 6" and CLE wafer
- Lower kerf loss
- Higher productivity
Edge rounding substantially reduces the chipping of the edges in subsequent process steps.

- Higher mechanical strength of the wafer
- Prevent the epi-crown (irregular outgrowth of silicon at the wafer edge)
- Prevent the piling up of photoresist at the edges
- Costumer specified edge length and arc
Ground process

Reduce surface damage and provide a good flatness for lapping procedure
The silicon wafers are lapped between two large counterrotating steel disks. About 30 µm – 40 µm from each wafer side will be removed.

- The wafers are held and led by a lapping carrier.
- A suspension of abrasive (powder of SiC, Al₂O₃ or a mixture of oxides) is added.
- GBIR (TTV) < 2 µm
Removal of particles and mechanical damage is the main purpose for etching wafers. Typically 15 µm – 20 µm from each wafer side are removed.

- A mixture of HF/HNO₃ is used.
- During the etching process the geometry parameters especially GFLR (TIR) should not change.
Different gettering mechanisms on Si Wafer

Impurities deposited during the IC-Process (Fe, Ni, Cu, Au et. al.)

Epitaxial layer

Silicon wafer

Mismatch

Defects

Polysilicon layer

Silicon-Nitride layer

Mech. backside treatment

Laser radiation

Ion-implantation

P-diffusion

Precipitates free zone (appr. 5µm)

Oxygen precipitates

Intrinsic gettering

Extrinsic gettering

Impurities deposited during the IC-Process (Fe, Ni, Cu, Au et. al.)
Polishing is a mechanical/chemical treatment using appropriate chemicals (SiO₂) and a polishing pad. For one-side polishing the wafers are mounted on plates and than polished face down on a rotating polishing plate.

The polished wafer surface must be free of any residual damage (stacking faults during subsequent oxidation treatments).

The surface flatness must lie within the depth of focus range of the optical system.

In final polishing haze will be removed and COP´s should be reduced (due to better GOI).

Reduction of micro-roughness (better yield in CMP process).

Mounting is particularly sensitive in this regard. Just one particle in the extremely thin layer of mounting wax causes a local elastic warping of the wafer.
From Sand to Silicon Wafer

Polishing

- Wafer production
- Wafer Cleaning
- Wafer Mounting
- Block Heating
- Ceramic Block Cleaning
- Demounting
- Wax Removal
- Final
- Intermediate
- Rough
- Block Cooling
Wax mounted wafers on a ceramic plate

3D of polished wafers

Typical values for a polished wafer:

- **Geometry** 8“ /µm
  - GBIR < 1.2
  - GFLR < 0.7
  - SFQRind < 0.07
  - SFQRmax < 0.13
**Pre-Cleaning**

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Modified RCA cleaning procedure</strong></td>
<td></td>
</tr>
<tr>
<td>SC-1</td>
<td>removal of organics and particles</td>
</tr>
<tr>
<td>DI Water</td>
<td></td>
</tr>
<tr>
<td>DHF</td>
<td>removal of native oxide film and metallic ions (exc. Cu, Al)</td>
</tr>
<tr>
<td>DI Water</td>
<td></td>
</tr>
<tr>
<td>SC-1</td>
<td>removal of organics and particles</td>
</tr>
<tr>
<td>DI Water</td>
<td></td>
</tr>
<tr>
<td>SC-2</td>
<td>removal of metallic ions, native oxide formation</td>
</tr>
<tr>
<td>DI Water</td>
<td>Final cleaning</td>
</tr>
</tbody>
</table>

View of a fully automatic pre-cleaning system
Final cleaning procedure

1. Rotor box (remove particles)
2. DI Water (spray system)
3. Spin dryer
4. Final inspection (visual, laser scan)
5. Epitaxy
6. Packaging

Detailed View of a final-cleaning system
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What's necessary in the future

- Due to lower device dimensions perfect silicon must become reality
- Defects in silicon crystal will be much more important → improve growth techniques
- Surface damage must be reduced → improve polishing techniques
- Micro-roughness must be improved → improve grinding/polishing techniques
- Metal contamination get more important to our costumers → improve the whole process, check the equipment material, use novel equipment materials, use purer chemicals, improve analytical methods
- Improve flatness → better polishing techniques (double side polishing, especially at 300 mm), novel polishing techniques, improve grinding
- Lower particel contamination especially lower size (> 0.065 µm) → crystal growth, polishing, cleaning, measurement equipment

- Further reduction of cost especially for 300 mm wafer → improve productivity, cycle time, process efficiency, yield, ...
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Kontaktadressen (www.siltronic.com)

Erich Nunweiler
Burghausen, Germany
Siltronic AG
Johannes-Hess-Straße 24
D-84489 Burghausen
Tel. ++49(8677)83-4335
Fax. ++49(8677)83-4172
E-Mail: Erich.Nunweiler@siltronic.com

Dr. Jörn Mittenzwei
Freiberg, Germany
Siltronic AG
Berthelsdorfer Straße 113
D-09599 Freiberg
Tel. ++49(3731)278-394
Fax. ++49(3731)278-233
e-Mail: Joern.Mittenzwei@siltronic.com

Tom Fahey
Portland, USA
Siltronic AG
7200 N.W. Front Avenue
P.O.Box 83180
Tel. ++1-503-219-7901
Fax. ++1-503-219-4606
E-Mail: Tom.Fahey@siltronic.com

Daniel Loh
Singapore
Siltronic AG
Tel. ++65-549-6121
Fax. ++65-549-6193
e-Mail: Daniel.Loh@siltronic.com

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